

LOCALIZED AND CMOS COMPATIBLE GROWTH OF CARBON NANOTUBES ON A $3 \times 3 \mu\text{m}^2$ MICROHEATER SPOT

Alain Jungen, Christoph Stampfer, Marc Tonteling, Sebastien Schiesser,

Debajyoti Sarangi, and Christofer Hierold

Micro and Nanosystems, ETH Zurich, Switzerland

e-mail: alain.jungen@micro.mavt.ethz.ch

ABSTRACT

We present the synthesis of carbon nanotubes utilizing a localized chemical vapor deposition method. The modified method relies on the usage of local heat sources defined in microscale resistive heaters through a standard polysilicon based surface micromachining process instead of a global reaction furnace heating. The presented method provides a remedy to amorphous carbon contamination of the exposed chip and most importantly a significant step towards the process integration of nanotubes into functional devices. Since the synthesis is carried out globally at room temperature the suggested process is compatible with standard CMOS technology. The presented fabrication method is batch-fabrication and thus complementary to discrete fabrication techniques and serves to build devices to evaluate the electromechanical properties of carbon nanotubes.

Keywords: Process integration, Localized growth, Carbon nanotubes, Nanosystems

INTRODUCTION

The electrical and mechanical properties of carbon nanotubes (CNTs) are extraordinary and have generated considerable excitement in the area of nanoscience and nanotechnology. Besides the unique and useful structural properties, a nanotube has high Young's modulus and tensile strength. A single-walled CNT can behave as a well-defined metallic, semiconducting or semi-metallic wire depending on two key structural parameters defined by the chirality vector (n, m) [1]. The relationship between nanotube atomic structures and electronic structures along with the fundamental question of how mechanical deformation affects the electrical properties are in the scope of research investigations.

For the synthesis of CNTs three different methods have been successfully employed in the past [1]. Arc-discharge and laser ablation methods produce CNTs in a bulky fashion and can only be integrated into microchips in a discrete manner [2]. The reaction product generally results in tangled nanotube bundles mixed randomly with various purities. Chemical vapor deposition (CVD) holds as the method of choice for

direct and batch-type synthesis of nanotubes into chips [3, 4]. Recent research on CVD growth has been driven by the idea that aligned and ordered nanotubes can be synthesized on surfaces with control. However this process lacks compatibility with chips presenting microelectronic circuitry like CMOS (melting of metal layers due to elevated temperatures). Their anticipated unmatched transducer performance makes CNTs valuable candidates for future sensor generations, thus the need for fully integrated chip compliance.

FABRICATION

Microheaters were made using a triple polysilicon layer surface micromachining foundry service (*PolyMUMPs*). They can be defined in any of the releasable polysilicon layers. The chip is acetone stripped and HF released before catalyst deposition. Fig. 1 shows an image of an uncoated released microheater.

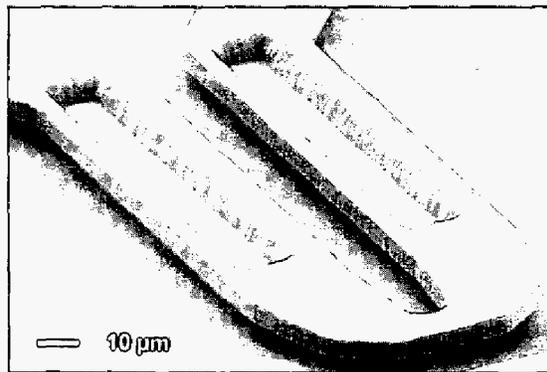


Fig. 1. Scanning electron microscopy (SEM) image of a typical (released) microheater.

The sample is now coated with a catalytic solution containing iron nitride, molybdenum and alumina nanoparticles dissolved in methanol [4]. The evaporation of the solvent is enhanced in air using a hot plate ($\sim 40^\circ\text{C}$). After evaporation the chip is die bonded onto a support chip containing large contact pads using non-permanent hot-wax and wire bonded (see inset of Fig. 2). The system is then transferred into

a vacuum chamber featuring electrical *in situ* connection. Please refer to Fig. 2.

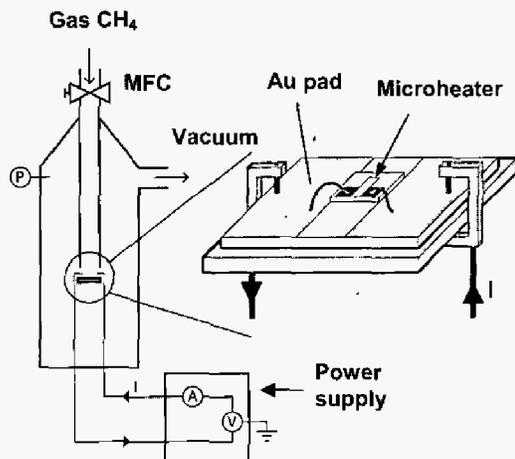


Fig. 2. Schematic of experimental setup for the fabrication process.

The vacuum chamber is first subjected to argon purge and evacuation cycles. Subsequently methane (CH_4) is fed at 150 sccm and the pressure is kept at 75 mbar. Heat is produced through resistive heating (Joule heating) by flowing electrical current through polysilicon beams. A voltage controlled power supply is used and simultaneous resistance monitoring is done. The reaction is carried out at the region of the generated heat during 15 min using increasing voltage steps in a non-linear resistivity regime (see Fig. 5).

RESULTS AND DISCUSSION

Fig. 3 shows carbon nanotubes locally grown directly on the microheater spot. Growth of small (< 20 nm) diameter nanotubes occurred in the vicinity of the maximum temperature. Bundles of single walled or thick multi walled CNTs were observed in colder regions away from the maximum heat spot.

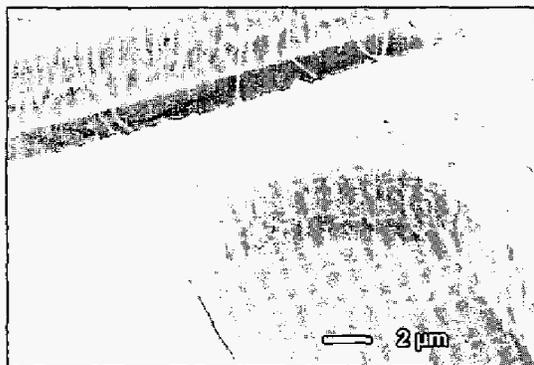


Fig. 3. SEM of microheater containing locally synthesized carbon nanotubes.

The growth mechanism, which has not been investigated here, is assumed to be identical to typical CVD growth of CNTs, namely involving the dissociation of methane catalyzed by the transition metal, and dissolution and saturation of carbon atoms in the metal nanoparticle. It is proposed that the precipitation of carbon from the saturated metal particle leads to the formation of tubular carbon solids in sp^2 structure [1].

A finite element analysis (FEA) electrothermal multiphysics (conductive media and heat transfer) model of the microheater was created using FEMLAB. For the simulation following assumptions were made. The anchors are ideal in the sense that they remain at ambient temperature at all times. The heat conduction from the freestanding bridge through the air gap ($2 \mu\text{m}$) to the substrate can be neglected. This assumption is acceptable as the heated surface is comparably small and, what is more, the air conduction reduces in a low pressure regime (below 100 mbar). Furthermore, buckling down of the microbridge due to compressive stress generated by thermal expansion as reported in reference [5] as to reduce the air gap distance and loose thermal energy to the substrate was not observed in the present experiment. Radiation and convection losses can be neglected. Calculations have shown that for the given system these losses are up to four orders of magnitude lower than the conduction losses.

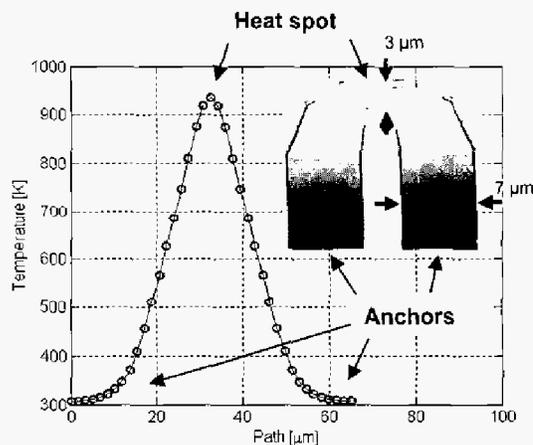


Fig. 4. FEMLAB simulation of the microheater tip. The plot shows the temperature distribution at an applied voltage of 5.5 Volts (DC) through the heater arm (anchor-tip-anchor). The inset shows the corresponding spatial temperature distribution. The slices represent isothermals.

The simulation results validate the presence of strong temperature gradients throughout the heater beams. The inset in Fig. 4 shows that the heat spot is constrained to approximately $3 \times 3 \mu\text{m}^2$ (see also Fig. 6 to confirm the dimensions of the square-shaped heat spot) and temperature gradients of $\sim 30 \text{ K } \mu\text{m}^{-1}$ were

achieved (excluding secondary effects which are discussed later in this text). The method of constraining heat generation to a localized spot enhances the position control of the CNT synthesis and the integration density of discrete nanotube based devices on a chip. Fig. 5 shows the I-V characteristic of the microheater. Complementary, the temperature of the heater spot (=max. temp.) is plotted as a function of the input voltage.

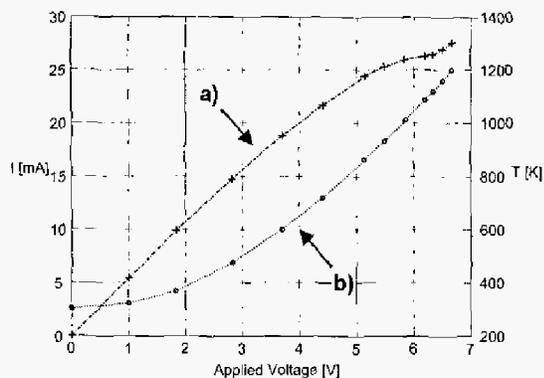


Fig. 5. a) I-V measurement of a microheater during the growth process (upper curve, '+' are measurement points). b) Simulated maximum temperature vs. applied voltage (lower curve, 'o' are simulation points).

Growth using methane as a carbon feedstock requires elevated temperatures (above 1100 K). Considering the simulation results, these high temperatures require the polysilicon to enter a non-linear resistivity regime. Doping concentrations have a significant impact on the temperature dependent electric resistivity within polysilicon. Furthermore, grain boundaries in polysilicon exhibit charge carrier trapping and contribute to the temperature dependent behavior. At high doping levels ($> 10^{19} \text{ cm}^{-3}$) electron and hole scattering from thermal vibrations dominate effects from increase in charge carrier concentration. The temperature dependent resistivity behavior is dominated by mobility [6]. Lattice and impurity scattering mobility (μ_L) and (μ_I) respectively, significantly contribute to charge carrier mobility at high temperatures [7]. The mobility terms are found to have the form

$$\begin{cases} \mu_L \propto T^a, & -2.7 < a < -1.5 \\ \mu_I \propto T^b, & 1.5 < b < 2 \end{cases} \quad (1)$$

From these considerations a temperature dependent resistivity model is taken to be

$$\rho(T) = a_1 + a_2 T^{a_3} \quad (2)$$

where the parameters a_i with $i \in \{1,2,3\}$ are extracted empirically. Fig. 6 shows the microheater which is just before failure due to melting. The heater burnt at an applied voltage of 7.5 V and the corresponding simulated temperature was about 1400 K. The difference to the theoretical melting point of silicon and polysilicon being 1710 K [8] is explained by the presence of super-local heating due to imperfections in the polysilicon microstructure. Failure is assumed to occur at grain boundaries as observed in Ref. [9].

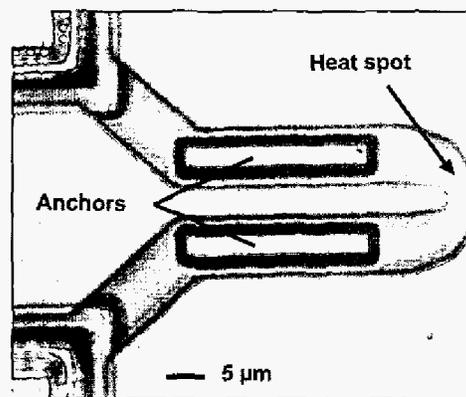


Fig. 6. Picture of the radiation of the heater. The temperature peak is centered. Applied voltage: 6 V at 100 kHz. The horizontal rectangular structures anchor the beams to the substrate.

Thomson effect, accounting to secondary effects, has to be taken into account due to the temperature gradient leading, in contrast to Fig. 4, to an off-centered temperature peak sensitive to the direction of the current. An AC signal can be used to smear out the temperature profile and to center the heat spot which can be seen in Fig. 6. Both, the increased current density due to a narrowed cross-sectional area of the heater beam and the presence of strong temperature gradients contribute to an amplified Thomson effect influencing the spatial position of the temperature peak.

Within the framework of a CMOS compatible process [11] not only the maximum process temperature but thermal budgets, taking into account both temperature and time, are also considered. A typical hydrogen annealing step at 700 K for 30 min (CMOS 0.5 μm technology generation) might already affect doping profiles but this is considered from a total process flow point of view. Additional process steps as proposed for a compatible integration of MEMS & CNTs should perform lower thermal budgets. Typical CVD processes for nanotube growth are run at 1175 K

for about 10 min. Additionally, heating and cooling ramps of 150 K min^{-1} and 30 K min^{-1} respectively are achieved with industrial 4-inch LPCVD furnaces. The resulting thermal budget is far beyond CMOS compatibility. Referring to Fig. 7, instantaneous heating ($\tau=0.01 \text{ ms}$) and very low power consumption ($\sim 200 \text{ mW}$, Fig. 5) are achieved.

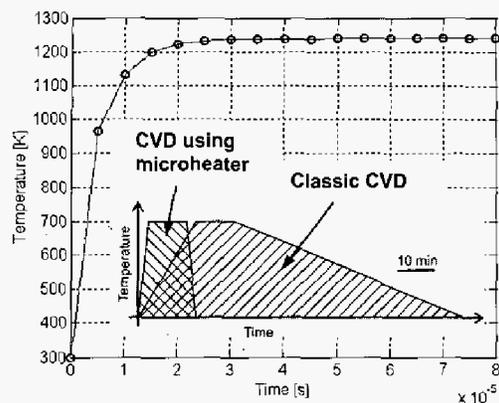


Fig. 7. Simulated thermal response of microheater. At time $t=0$ the heater was fed with 7.1 Volts (DC) and the transient analysis yielded a thermal constant of $\tau=0.01 \text{ ms}$. Inset: Comparison of thermal budgets between conventional and microheater CVD processes.

CONCLUSION AND OUTLOOK

We demonstrated the synthesis of carbon nanotubes utilizing a localized chemical vapor deposition method relying on the usage of local heat sources defined in microscale resistive heaters. The presented method provides a remedy to amorphous carbon contamination of the exposed chip and most importantly a significant step towards the process integration of nanotubes into functional devices. Since the synthesis was carried out globally at room temperature the suggested process is compatible with standard CMOS technology. Simulation results yielded the presence of strong temperature gradients throughout the microheaters enabling high density nanotube integration processes. Thermal budgets have been lowered compared to classic thermal CVD.

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